

ULTRAVIEW

THE NEW LEADER IN
DATA ACQUISITION

Designed to address requirements for the highest-performance data acquisition systems.

Applications

- ▶ Military
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Ultraview Corporation

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PCIe ADC DAQ

AD14-400

High-Speed Data Acquisition Boards

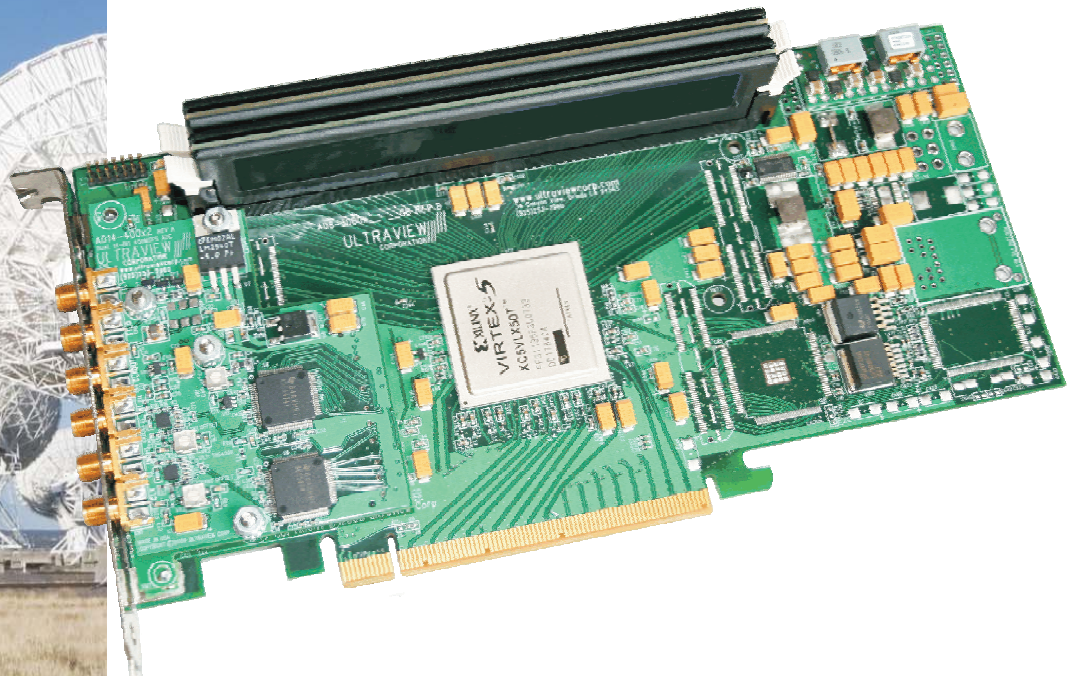
NEW!

- ▶ **14-bit resolution**
- ▶ **Up to 400MSPS**
- ▶ **Deep on-board RAM – Up to 8GB**
- ▶ **Customizable – On-board FPGA allows reconfigurable signal processing and ultra-deep recording**
- ▶ **Ultra Fast Data Transfer to Host – Typically 1GB/sec, depending on system**
- ▶ **One or two channels**
- ▶ **OEM customization available**

The AD14-400 is Ultraview's latest series of state-of-the-art PCIe high-speed data acquisition (DAQ) boards. The line features uninterrupted acquisition of one or two concurrent 400MSPS 14-bit A/D channels.

When installed in a PCIe x16 slot, the AD14-400 acquires data at an aggregate rate of up to 800MSPS, optionally process it with the on-board FPGA, buffer it into the on-board 8GB RAM, and continuously stream the data to host system RAM at up to 1.4GB/sec for immediate user processing, graphical display, or storage to disk.

External triggering and selective recording features allow acquisition to be dynamically stopped and started in response to TTL inputs, increasing effective memory depth by storing only the desired data.



Ultraview's AD14-400 is the new benchmark with which all other 14-bit data acquisition boards will be compared.

Rapid development and OEM-customization

Designed for high-speed, low-jitter operation in critical OEM applications, the AD14-400 allows either straight data acquisition, requiring no user development, or real-time FPGA dataflow processing using the on-board Xilinx Virtex-5™ (XC5VLX50T™).

For use as a standard DAQ board, the supplied user software and device driver allow users to acquire and view data with only a few minutes required to set up the board. Drivers, user software, and example user source code are supplied for both 64-bit Linux and 32-bit Windows Vista™/XP™. LabVIEW drivers are under development. Graphical waveform display software and routines to store data to disk are included with all boards in C-language source and in ready-to-run executable form.

The AD14-400's host-uploadable firmware feature lets users reconfigure the on-board FPGA through the host system's PCIe bus, without a programming cable. This allows users to quickly, and even remotely, modify the board's supplied data acquisition VHDL firmware to perform advanced application-specific hardware signal processing, including filtering, sub-band tuning, averaging, spectroscopy, SDR, and image processing. This modular VHDL firmware source is available to OEM users.

Modular front-end mezzanines

For OEM applications, user- or Ultraview-designed front-end mezzanines may be attached to the board, including higher resolution A/D and D/A converters, filters, amplifiers, and mixers.

Ultra-fast multi-board, multi-channel data acquisition

Multiple AD14-400 boards may be ganged to be simultaneously triggered. For example, with four AD14-400x2-8GBs and a SPLIT4/8B clock/trigger splitter, eight A/D channels can be acquired concurrently at 400MSPS per channel, for a 3200MSPS aggregate rate, with 4GB of acquisition depth on each channel.

The boards support external clocks of 10MHz to 400MHz (sampling rates of 10MSPS to 400MSPS), and also have an optional 400MHz internal clock (other frequencies available).

Ordering info

AD14-400x1-4GB	14-bit ADC, 10MSPS-400MSPS, one channel, 4GB RAM, XC5VLX50T FPGA
AD14-400x1-8GB	14-bit ADC, 10MSPS-400MSPS, one channel, 8GB RAM, XC5VLX50T FPGA
AD14-400x2-4GB	14-bit ADC, 10MSPS-400MSPS, two channel, 4GB RAM, XC5VLX50T FPGA
AD14-400x2-8GB	14-bit ADC, 10MSPS-400MSPS, two channel, 8GB RAM, XC5VLX50T FPGA

Specifications, configurations, and availability are subject to change without notice.

Specifications

Driver OS support:

- ▶ RedHat Linux WS5.0 64-bit
- ▶ Centos 5.3 64-bit
- ▶ Windows Vista/XP 32-bit
- ▶ LabVIEW (TBA)

A/D converter resolution: 14-bit

Signal-to-noise ratio: 68dB

Analog input range: -350mV to +350mV (may not exceed 800mV)

Analog input impedance:

50Ω || 2pF

Analog input bandwidth:

DC to 1.1GHz minimum (-3dB bandwidth)

Sampling rate into on-board

RAM: 400MSPS max, 20MSPS min

Optional clock input AC voltage

range: 0.2V peak-to-peak min, 1.0V peak-to-peak max (may not exceed ±5V)

Clock input impedance:

50Ω in series with 0.01μF

Optional external trigger input:

TTL

Optional selective recording input

and low-speed Xilinx ADC input: 0V-3.0V (may not exceed 3.2V)

Peak DMA transfer rate to host-system RAM: Up to 1.4GB/sec (depends on system)

On-board RAM:

4GB or 8GB DDR-II

Operating temperature:

0 to 50°C or 32 to 122°F

Storage temperature: -25 to 85°C or -13 to 185°F

Airflow: Minimum 100 lf/minute

Power requirements (board occupies two slots):

- ▶ +3.3V ±5% @ 3.3A max (2.6A typical)
- ▶ +12V ±5% @ 2.0A max for 4GB, 2.5A max for 8GB

Size: 10.7 cm x 21.9 cm or 4.2 in. x 8.625 in.

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